

**Dr. Suraj Kumar Saw**  
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Add: Lower Rajbari Road Near Model School  
Jharia, Dist- Dhanbad Jharkhand pin 828111  
Mob No- 8416002238/7870131734

## **Teaching and Research experience: (5 years)**

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- **Teaching Assistant**

Jan. 2020 - Jun. 2020

*Indian Institute of Information Technology Surat Gujarat*

Subject taught:

- Digital VLSI Design
- Digital logic Design
- Microcontroller

- **SRF under SMDP C2SD Project Meity Govt. of India**

Mar 2018 - Jan. 2020

*National institute of Technology- Arunachal Pradesh India*

Work-1

- CML based prescaler circuits in dual mode analysis
- Worked on synthesis, Simulation and physical layout
- Technology: 90nm/28nm UMC
- Tools: Virtuoso, Calibre, PEX

Work-2

- A design approach of higher oscillation VCO made of CS amplifier
- Detailed mathematical modeling, simulation and post layout Verifications
- Technology: 90nm/28nm UMC
- Tools: Virtuoso, Calibre, PEX

- **JRF under SMDP C2SD Project Meity Govt. of India**

Mar 2016 - Mar. 2018

*National institute of Technology- Arunachal Pradesh India*

Work-1

- A power efficient charge pump circuit configuration for fast locking PLL application
- Worked on monte carlo, corner analysis, Mismatch etc.
- Technology: 90nm/28nm UMC
- Tools: Virtuoso, Calibre, PEX

Work-2

- PVT Aware Design of a Dead-Zone Free High Speed Phase Frequency Detector
- mathematical modeling, lock-in-time, Reset time and blind zone estimation
- Comparison with prior art with zero dead zone is achieved
- Technology: 90nm/28nm UMC
- Tools: Virtuoso, Calibre, PEX

- **Assistant Professor**

Aug. 2015 - Feb. 2016

*St Mary Technical campus Kolkata West Bengal*

Subject taught:

- Microprocessor
- Basic electronics

## **Technical Skills**

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- Hardware Languages : Verilog HDL and SystemVerilog
- HDL and HVL
- Sequential Languages: Basic C,
- Operating Systems: Red Hat Enterprise Linux v7, CentOS v7, Windows 7/10
- EDA Tools and Technologies : Cadence Design Systems:, Virtuoso IC6.1.6,
- Mentor Graphics: Calibre 2016.114;
- Synopsys: Design Compiler, HSPICE L-2016.3, Design Vision
- Xilinx: Xilinx ISE Design Suite 14.5/14.7
- Tanner EDA: Tanner 7 (L-Edit, S-Edit, T-Spice)
- Linear Technology: LT-Spice
- Others : Matlab R2017a, Origin 9.4, Microsoft office, Excel

## **Educational Qualification**

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<b>Examination</b>	<b>Institute</b>	<b>University</b>	<b>Year</b>	<b>CGPA</b>
Ph.D Specialization VLSI Design (ECE)	National Institute of technology Arunachal Pradesh India	National Institute of technology Arunachal Pradesh India	2020	9.50/10
PG Specialization Master in Engineering	Birla Institute of technology Mesra Ranchi	Birla Institute of technology Mesra Ranchi	2015	8.35/10
UG Specialization B.Tech (ECE)	CIT Tatisilwai Ranchi	Ranchi University Ranchi	2013	8.30/10

## **Activities and Honors:**

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- Secured first position in b tech 3rd and 8th semester examination in our branch
- IEEE Student Membership since March 2015(Membership No 93353307)
- Associate Member of Indian society of VLSI education Ranchi

## **Additional Skills:**

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- Completed 21 days vocational training from ARTTC BSNL, RANCHI
- A 10 days workshop on winter school digital VLSI design
- A Master Thesis report on “Design of low power CMOS VCO for wireless applications”

## Selected Publications:

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### Journals (8 SCI Indexed)

- Alak Majumder, Monalisa Das, Suraj Kumar Saw, Abir J. Mondal, and Bidyut K. Bhattacharyya. "Variation Aware Design of 50-Gbit/s, 5.027-fJ/bit Serializer Using Latency Combined Mux-Dual Latch for Inter-Chip Communication." *IEEE Transactions on Circuits and Systems I: Regular Papers* 66, no. 3 (2018): 1231-1244. DOI: 10.1109/TCSI.2018.2877571 (I.F 3.934)
- Suraj Kumar Saw, Madhusudan Maiti, Preetisudha Meher and Alak Majumder. "PVT Aware Design of a Dead-Zone Free High Speed Phase Frequency Detector in 90nm CMOS." *Recent Advances in Electrical & Electronic Engineering, Bentham science publications* (2018). DOI: 10.2174/2352096512666190314111752
- Suraj Kumar Saw, Payali Das, Madhusudan Maiti, and Alak Majumder. "A power efficient charge pump circuit configuration for fast locking PLL application." *Microsystem Technologies Springer* (2018) DOI: 10.1007/s00542-018-4037-5. (I.F 1.737)
- Suraj Kumar Saw, Sandeep Kumar Yadav, Madhusudan Maiti, Abir Jyoti Mondal and Alak Majumder "A design approach of higher oscillation VCO made of CS amplifier with varying active load" *Microsystem Technologies Springer* (2019) DOI: 10.1007/s00542-019-04500-5. (I.F 1.737)
- Madhusudan Maiti, Suraj Kumar Saw, Vijay Nath, and Alak Majumder. "A power efficient PFD-CP architecture for high speed clock and data recovery application." *Microsystem Technologies Springer* (2019) pp. DOI: 1-10.10.1007/s00542-019-04458-4 (I.F 1.737)
- Maiti, Madhusudan, Anupama Paul, Suraj Kumar Saw, and Alak Majumder. "Passive element free variation aware decision circuit for 40 Gb/s CDR application." *Microsystem Technologies Springer* (2019) pp. 1-9. DOI: 10.1007/s00542-019-04683-x (I.F 1.737)
- Maiti, Madhusudan, Suraj Kumar Saw, Abir jyoti mondal and Alak Majumder "A hybrid design approach of PVT tolerant, power efficient ring VCO" *Ain Shams Engineering Journal, Elsevier* November 2019 DOI: 10.1016/j.asej.2019.10.009 (I.F 3.091)
- A. Majumder, M. Das, Suraj Kumar Saw, B.K. Bhattacharyya, "An Energy Efficient PVT Aware Novel CML-TG based Mux-Latch Circuit Serializes High Rate Data", *Microsystem Technologies, Springer*, 2018 DOI: 10.1007/s00542-018-4093-x (I.F 1.737)

## Conferences

- Suraj Kumar Saw, Preetisudha Meher, and Swarnendu Kumar Chakraborty. "Design of high frequency D flip flop circuit for phase detector application." In TENCON (2017) IEEE Region 10 Conference, pp. 229-233 DOI: 10.1109/TENCON.2017.8227867
- Suraj Kumar Saw, Payali Das, Madhusudan Maiti, and Alak Majumder. "A 90nm Design of Charge Pump Circuit for Perfect Current Matching" In 6th International Conference on computing, communication and sensors networks. (2017) Vol. I pp 128-132.
- Suraj Kumar Saw, Madhusudan Maiti, Preetisudha Meher, and Swarnendu Kumar Chakraborty. "Design and implementation of TG based D flip flop for clock and data recovery application." IET Digital Library International Conference on Recent Trends in Engineering, Science & Technology (2016): 23-3 DOI: 10.1049/cp.2016.1491.
- Payali Das, Suraj Kumar Saw, and Preetisudha Meher. "Design of Differential Amplifier Using Current Mirror Load in 90 nm CMOS Technology" In Information Systems Design and Intelligent Applications, pp. 421-429. Springer, Singapore, (2019) DOI: 10.1007/978-981-13-3329-3\_39

## List of References:

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- Dr. Preetisudha Meher  
Assistant Professor, Electronics and Communication Engineering  
Email id: preetisudha@nitap.ac.in  
Contact No: +91-9438823600, 9040544300
- Dr. Alak Majumder  
Assistant Professor, Electronics and Communication Engineering  
Email id: alak@nitap.ac.in  
Contact No: +91-9436288578

## Personal Details:

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- Date of Birth : January 14, 1990
- Father's Name : Subodh Kumar Saw
- Gender : Male
- Marital Status : Married
- Nationality : Indian

Date: 26-08-2020  
Place: Surat Gujarat

Dr. Suraj Kumar Saw