**Profile of Faculty**

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| **i** | **Name** | Dr. Satish S. Narkhede |  |
| **Ii** | **Date of Birth** | 12 – 08 – 1964 | |
| **iii** | **Education Qualifications** | • BE (Ind ELEX)<br>• ME (E&TC)<br>• Ph.D. (E&TC) | |
| **iv** | **Work Experience** | | |
| | • **Teaching** | 30 years | |
| | • **Research** | | |
| | • **Industry** | -- | |
| | • **Others** | -- | |
| **v** | **Area of Specialization** | • Semiconductor devices and circuits,<br>• Multi-valued Logic,<br>• Microelectronics | |
| **vi** | **Courses taught at Under Graduate/ Post Graduate Level** | • Electronics Devices and Circuits<br>• Integrated Circuits and Applications<br>• Control systems<br>• Network Synthesis | |
| **vii** | **Research guidance** | -- | |
| | • **No. of papers published in National/ International Journals/ Conferences** | 20 Publications | |
| | • **Master** | Guided 16 students for ME | |
| | • **Ph.D** | -- | |
| **viii** | **Projects Carried out** | 02 Funded projects<br>• Design and Fabrication of CMOS Ternary Logic Gates" (2007-09) Rs. 2,00,000/- (Two Lakhs Only) SPPU, Pune<br>• Reconfigurable FPGA"(2008-10) Rs. 2.50,000/- (Two Lakhs and Fifty Thousand Only) SPPU, Pune. | |
| **ix** | **Patents** | -- | |

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|---|---|---|
| **x** | **Technology Transfer** | -- |
| **xi** | **Research Publications** | Please refer to the appended details |
| **xii** | **No. of Books published with details** | Please refer to the appended details |

**BOOKS PUBLISHED WITH DETAILS**

| Sr. No . | Name of the Authors | Title of the Book | Year |
|---|---|---|---|
| 1. | Mr. Narkhede S. S<br>Mr. Mundada G. S. | Digital Electronics and Logic Design | July 2005 |
| 2. | Mr. Narkhede S. S<br>Mr. Mundada G. S. | Semiconductor Devices and Circuit | July 2005 |
| 3. | Mr. Narkhede S. S<br>Mr. Mundada G. S.<br>Mr. Y. Ravinder | Digital systems | July 2005 |
| 4. | Mr. Narkhede S. S<br>Mr. Mundada G. S. | Electronics Devices and applications | July 2005 |

**PAPERS PUBLISHED IN NATIONAL/ INTERNATIONAL JOURNALS/ CONFERENCES**:

1. Narkhede S. S., Chaudhari B. S., Kharate G. K, "An Efficient MIFGMOS Transistor Based Design Of Ternary ALU Using Novel Ternary Level Shifter" Journal of Information Processing System, Computer Systems and Theory, South Korea (submitted in June , 2015)
2. Narkhede S. S., Chaudhari B. S., Kharate G. K, "A Novel Hybrid MIFG-CMOS Based Approach For The Realization of Ternary Gates" ICTACT Journal on Microelectronics, vol.01, issue 2, 2015, pp. 45-56
3. Narkhede S. S., Chaudhari B. S., Kharate G. K, "Design and Implementation of Efficient Ternary Control Unit". Journal of VLSI Design Tools and Technology (Scientific Technical Medical , STM Journal), vol. 5 issue 3, 2015, pp. 55-70
4. Narkhede S. S., Kharate G. K, Chaudhari B. S., "Design and Implementation of an Efficient Instruction Set for Ternary Processor" International Journal of Computer Application, 83.16, 2013, pp. 33-39.
5. Narkhede S. S., Chaudhari B. S., Kharate G. K, "A VHDL Implementation of Ternary Arithmetic and Logic Unit for Multi Valued Processor" CiiT PDCS, vol 7, no. 6, 2015 pp.185-193
6. Dhande A. P., Narkhede S. S,. Dudam S. S., VLSI Implementation Of Ternary Gates Using Tanner Tool" 2nd IEEE International Conference on Devices, Circuits and Systems (ICDCS), 2014, Coimbatore, pp. 1-5

7. M.N. Kishor, S.S. Narkhede, Design of a ternary FinFET SRAM cell, Symposium on Colossal Data Analysis and Networking (CDAN), 2016
8. Perni Venu Gopal ; Satish Narkhede ; G. Sasikala, Implementation of ternary logic gates using FGMOS, 2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM), 2015
9. Priyesh Parikh ; Satish Narkhede, High performance implementation of mixing of column and inv mixing of column for AES on FPGA, International Conference on Computation of Power, Energy Information and Commuincation (ICCPEIC),2016
10. R.S.Bodhe, S.S.Narkhede, Shirish Joshi, "Performance Comparison of FFT and DWT based OFDM and Selection of Mother Wavelet for OFDM**"** International Journal of Computer Science and Information Technologies (IJCSIT), ISSN: 0975-9646, Vol. 3(3), 2012, 3993-3997, Tech Science Publications, Chidambaram, and Tamilnadu, India.
11. R.S.Bodhe, S.S.Narkhede, Shirish Joshi, "Design of Simulink Model for OFDM and Comparison of FFT-OFDM and DWT-OFDM" International Journal of Engineering Science and Technology (IJEST), ISSN: 0975-5462, Vol. 4 No. 05 May 2012, Page No.1914-1924,
12. G. V. Chaudhari, S. S. Narkhede, "Desing of DGS microstrip antenna with Array structure ground plane", ePGCON2012, Pune.
13. Anumeha Zanjal and S.S Narkhede, "Design And Frabrication of Fractal Shaped Microstrip Band Pass Filter (Synthetic Aperture Radar Application)" National Conference on Sensor Networks and Embedded Systems (NCSNES-2011), Abasaheb Garware College, Pune
14. Anumeha Zanjal and S.S Narkhede, "Design And Frabrication of Fractal Shaped Microstrip Band Pass Filter (Synthetic Aperture Radar Application)" ePGCON-April 2011, MIT Pune.
15. Yogita Azar, S.S Narkhede " System on chip FIR filter using partial Reconfiguration platform" Feb 2010, Father C Rodrigues Institute of Technology washi , National conference on nascent technology, 2010
16. Yogita Azar, S.S Narkhede, "Partial reconfiguration of FPGA at run time " National conference on pervasive computing 2010, Sinhgad
17. Yogita Azar, S.S Narkhede, "Dynamic partial reconfiguration of FPGA, used in matrix multi for area and time efficiency, National conference on pervasive computing 2010, Sinhgad
18. Arundhati S.Dhampalwar, Mr.S.S.Narkhede," A SOC for Matrix Inversion Using Dynamic Partial Reconfiguration of FPGA", NCPC-2010,at Sinhgad College of Engineering,Vadgaon Pune ,9-10 APR 2010.
19. Arundhati S.Dhampalwar, Mr.S.S.Narkhede," A System on a chip FIR Filter using Partial Reconfiguration Platform", NCNTE-2010, at Fr.C.Rodrigues Institute of Technology, Thane, 20-21 Jan 2010.
20. Arundhati S.Dhampalwar, Mr.S.S.Narkhede, " A reconfigurable digital filter based on partial reconfiguration of FPGA," iCost 2011 International Conference On Sunrise Technologies at SSVPS B. S. Deore College of Engineering Post Vidyanagri, Dhule, Maharashtra , 13-15 Jan 2011.

21. Arundhati S.Dhampalwar, Mr.S.S.Narkhede, “A Reconfigurable FIR Filter Design Using DPR Of FPGA,” ICSSA-2011 at G. H. Patel College of Engineering & Technology, Vallabh Vidhyanagar., Anand, Gujarat pp.118, 24-25 Jan,2011.